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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,475	07/23/2003	Bow-Yaw Wang	CA7038392001	1298
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BINGHAM, MCCUTCHEN LLP THREE EMBARCADERO CENTER 18 FLOOR SAN FRANCISCO, CA 94111-4067			EXAMINER ROSSOSHEK, YELENA	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/626,475

Applicant(s)

WANG, BOW-YAW

Examiner

Helen Rossoshek

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>06/30/2005</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to the Application 10/626,475 filed 07/23/2003 and amendment filed 06/13/2005.

2. Claims 1-30 remain pending in the Application. Claim 31 has been cancelled.

3. Applicant's amendment has been fully considered. Examiner finds it not persuasive.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1-30 are rejected under 35 U.S.C. 102(a) as being anticipated by Sheeran et al. ("Checking safety properties using induction and a SAT-Solver", November 2000, In Proc. Conference on Formal Methods in Computer-Aided Design).

With respect to claim 1 Sheeran et al. teaches a method of circuit verification (Introduction, Page 108), comprising: (a) performing bounded verification on a circuit design for a number of transition within FPGA verification (Abstract) using bounded model checking (Page 112) using finite state machine M with initial states I and state **transition T** (Pages 108, 111), wherein T is a transition relation on the set of states S assuming that the domain of T is the entire set of states S and repeatedly applying (number of transitions) the transition relation T to reach a state to satisfy P (property) (Page 111); (b) performing induction proof of a first property for the number of

Art Unit: 2825

transitions, wherein the induction proof is performed by a process within the inductive shape of proof the property P for each state S (Page 115) within applying the transition relation T a number of times leading to the state S satisfying property P (Page 111), comprising the acts of: including, in an inductive set of one or more states, a plurality of states of a circuit design, wherein the inductive set of one or more states includes at least states passing a first property of the circuit design (Page 108); transitioning by at least one step, in a forward direction, states of the inductive set passing at least the first property of the circuit design, resulting in transitioned states as shown on the Fig. 2, which depicts a state transition diagram for a circuit shown on the Fig. 1 (Page 109); determining if the transitioned states of the inductive set pass at least the first property of the circuit design by considering the reachable states, which are held by property P (states, which passed or satisfied property P) (Page 109); repeating at least the transitioning and determining, until at least, the determining results in the transitioned states of the inductive set passing at least the first property of the circuit design by starting in an initial state and repeatedly applying the transition relation always leads to a state satisfying (passing) property P (Page 111); (c) if the at least one property is not verified, then increasing a limit for the bounded verification and repeating from (a) by performing the induction-based method of checking the property P by applying the transition relation T **the number of times** leading to the state S satisfying property P (Page 111).

With respect to claims 2-11 Sheeran et al. teaches:

Claim 2: if all the transitioned states of the inductive set are determined to pass at least the first property of the circuit design, all the transitioned states of the inductive set determined to pass at least the first property of the circuit design were transitioned by a first total of transitions within determining a P-safe system wherein P-safe system is the system where all reachable states are P-states, which means that all states satisfy (pass) P (property) (Page 108);

Claim 3: transitioning, in forward direction, initial states of the circuit design by at least the first total of transitions, resulting in a forward transitioned set of states as shown on the Fig. 2 (top row), wherein property holds for all of the reachable states and wherein transitions are in forward direction as shown by arrows (Page 109);

Claim 4: if the forward transitioned set of states passes the first property of the circuit design, determining the circuit design to be formally verified for at least the first property of the circuit design within the method of the verification real FPGA by using the induction-based methods of safety property checking (Page 108);

Claim 5: the determining does not consider transitioned states resulting from transitioning of states of the inductive set failing at least the first property of the circuit design by checking systems for P-safety and generating a trace when the system turns out not to be P-safe assuming that the domain of T is the entire set of states S, so every state has a successor through T (Page 111);

Claim 6: the determining considers only transitioned states resulting from transitioning of states of the inductive set passing at least the first property of the circuit design as described in the Formulating the Problem (2.2) on the Page 111);

Claim 7: the transitioning is not performed on states of the inductive set failing at least the first property of the circuit design assuming that the domain of T is the entire set of states S, so every state has a successor through T (Page 111);

Claim 8: the transitioning is performed only on states of the inductive set passing at least the first property of the circuit design as shown on the Fig. 2 (Page 109);

Claim 9: each time the transitioning and the determining are repeated prior to transitioning, the inductive set includes transitioned states within the ability of the system to find the condition when the property is satisfied by going in loop (iteratively) (Page 112);

Claim 10: each time the transitioning and the determining are repeated, prior to transitioning, the inductive set includes transitioned states passing at least the first property of the circuit design (Page 112);

Claim 11: each time the transitioning and the determining are repeated, prior to transitioning, the inductive set excludes transitioned states failing at least the first property of the circuit design as shown in Algorithm 1 for checking if system is P-safe, wherein the programming code (function) returns only "True" condition in the end, wherein "True" condition is only satisfaction of the property P excluding failed states (Page 112).

With respect to claim 12 Sheeran et al. teaches: a method of circuit verification (Introduction, Page 108), comprising: (a) performing bounded verification on a circuit design for a number of transition within FPGA verification (Abstract) using bounded model checking (Page 112) using finite state machine M with initial states I and state

Art Unit: 2825

transition T (Pages 108, 111), wherein T is a transition relation on the set of states S assuming that the domain of T is the entire set of states S and repeatedly applying (number of transitions) the transition relation T to reach a state to satisfy P (property) (Page 111); (b) performing induction proof of a first property for the number of transitions, wherein the induction proof is performed by a process within the inductive shape of proof the property P for each state S (Page 115) within applying the transition relation T a number of times leading to the state S satisfying property P (Page 111), comprising the acts of: transitioning by at least one step, in a backward direction, states of an inductive set of at least one or more states of a circuit design passing at least a first property of the circuit design, resulting in transitioned states by working backwards through T when starting in a state violating property P as described in the section (2.2) Formulating the Problem on the Page 111; determining if the transitioned states of the inductive set fail at least the first property of the circuit design (Page 111); repeating the transitioning and the determining, until at least, the determining results in the transitioned states of the inductive set failing at least the first property of the circuit design by assuming that every state has a successor through T, so there are always loops (iteration) (Page 112); (c) if the at least one property is not verified, then increasing a limit for the bounded verification and repeating from (a) by performing the induction-based method of checking the property P by applying the transition relation T **the number of times** leading to the state S satisfying property P (Page 111).

With respect to claims 13-28 Sheeran et al. teaches:

Claim 13: a first iteration of transitioning by at least one step, in the backward direction, states of a first iteration of an inductive set of at least one or more states failing at least the first property of the circuit design, resulting in a first iteration of transitioned states (Page 112);

Claim 14: performing a first iteration of determining if the first iteration of transitioned states of the inductive set produce at least one state failing at least the first property of the circuit design (Page 112);

Claim 15: after the first iteration of transitioning, prior to the transitioning, the inductive set includes the first iteration of transitioned states within the Algorithm 1 to show an example of programming function to program the circuit design verification Bounded Model Checking using iteration and satisfiability check (Page 112);

Claim 16: after the first iteration of transitioning, prior to the transitioning, the inductive set includes the first iteration of transitioned states passing at least the first property of the circuit design (Page 112);

Claim 17: after the first iteration of transitioning, prior to the transitioning, the inductive set excludes the first iteration of transitioned states failing at least the first property of the circuit design by creating the programming function (code) within returning "True" if the system is P-safe and an "error trace" if not (Page 113);

Claim 18: at least after a first iteration of transitioning, the determining does not consider transitioned states resulting from transitioning of states of the inductive set failing at least the first property of the circuit design by using algorithm 2 shown on the Page 114 wherein states which failed to satisfy property P are excluded;

Claim 19: at least after a first iteration of transitioning, the determining considers only transitioned states resulting from transitioning of states of the inductive set passing at least the first property of the circuit design (Page 114);

Claim 20: at least after a first iteration of transitioning, the transitioning is not performed on states of the inductive set failing at least the first property of the circuit design (Page 114);

Claim 21: at least after a first iteration of transitioning, the transitioning is performed only on states of the inductive set passing at least the first property of the circuit design within the Algorithm 2 shown on the Page 114, wherein the text of the programming code of the verification of the circuit design shows the returning of the value of the transitioning performed only on states after the satisfaction of the property by states has been confirmed;

Claim 22: at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set includes transitioned states as shown in the Algorithm 2 on the Page 114;

Claim 23: at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set includes transitioned states passing at least the first property of the circuit design as shown in the Algorithm 2 on the Page 114;

Claim 24: at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set excludes transitioned states failing at least the first property of the circuit design as shown in the Algorithm 2 shown

Art Unit: 2825

on the Page 114, wherein the state which is not satisfied property P is not considered in the further consideration;

Claim 25: at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set excludes transitioned states able to reach, in one forward transition, any state of the circuit design failing at least the first property within forward and backward directions excluding the states which are not satisfied property P (Page 114);

Claim 26: at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set includes transitioned states except for transitioned states to reach, in one forward transition, any state of the circuit design failing at least the first property within forward and backward directions excluding the states which are not satisfied property P (Page 114);

Claim 27: at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set includes transitioned states passing at least the first property of the circuit design except for transitioned states able to reach, in one forward transition, any state of the circuit design failing at least the first property within forward and backward directions excluding the states which are not satisfied property P (Page 114);

Claim 28: at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set excludes transitioned states failing at least the first property of the circuit design and transitioned states able to reach, in one forward transition, any state of the circuit design failing at least the first

Art Unit: 2825

property as shown in the Algorithm 4 on the Page 115 by removing the dependence between iterations.

With respect to claims 29 and 30 Sheeran et al. teaches: a method of circuit verification (Introduction, Page 18), comprising: attempting bounded verification of one or more properties of a circuit design for at least a first predetermined number of transitions within Bounded Model Checking (Page 112) using finite state machine M with initial states I and state **transition T** (Pages 108, 111), wherein T is a transition relation on the set of states S assuming that the domain of T is the entire set of states S and repeatedly applying (number of transitions) the transition relation T to reach a state to satisfy P (property) (Page 111); attempting induction proof of the one or more properties of the circuit design for at least the first number of transitions (Introduction, Page 108); and determining if the one or more properties of the circuit design are verified, based at least on the bounded verification and the induction proof (Page 112); and if the bounded verification and the induction proof are insufficient to determine the one or more properties of the circuit design to be verified, increasing the first predetermined number of transitions by performing the induction-based method of checking the property P by applying the transition relation T **the number of times** leading to the state S satisfying property P (Page 111); repeating at least of attempting bounded verification and attempting induction proof by dividing the problem into sub-problems and working as loop-free states, but putting this loop-free states together and getting eventually loop (Page 112); and determining if the one or more properties of the

Art Unit: 2825

circuit design are verified, based at least on repeating, with the increased first number of transitions, at least one of bounded verification and the induction proof (Page 112).

Remarks

6. In the remarks of the Applicant's amendment applicant argues in substance:

A: The Sheeran reference fails to make any mention, or reaching of any increase in a limit of the bounded verification, wherein an increase based on failure to verify a property.

B: There is no teaching that "i" is a limit of a bounded verification.

C: The Sheeran reference does not anticipate, teach or suggest predetermined number of transitions.

7. Examiner respectfully disagrees for the following reasons:

As to A: Sheeran discloses FPGA verification (Abstract) within bounded model checking (Page 112) using finite state machine M with initial states I and state **transition T** (Pages 108, 111), wherein T is a transition relation on the set of states S assuming that the domain of T is the entire set of states S and **repeatedly** applying (number of transitions) the transition relation T to reach a state to satisfy P (property) (Page 111), wherein the inductive shape of proof the property P for each state S (Page 115) is performed within applying the transition relation T a number of times leading to the state S satisfying property P (Page 111).

As to B: Sheeran discloses that $i \geq 0$ and if the property P is violated somewhere in the reachable states an "i" will be found, for which the property is satisfiable (Page

112), wherein the transition relation T is copied i times (Page 110) and wherein the design circuit verification is performed using bounded model checking (Page 112).

As to C: Sheeran discloses setting T as a transition relation on the set of states S , wherein the domain of T is the entire set of states S and every state has a successor through T (Page 111), and repeatedly applying the transition relation always leading to a state satisfying property P (Page 111), wherein FPGA core verification is performed using BMC (bounded model checking) including property checking algorithm (Page 124).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

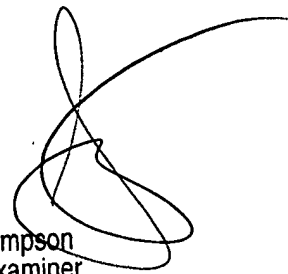
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

Art Unit: 2825

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A handwritten signature in black ink, appearing to be 'A. M. Thompson', written over the printed name.

A. M. Thompson
Primary Examiner
Technology Center 2800